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EXAMINER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
Office Action Summary	10/004,765	SAXENA, RAHUL
	Examiner	Art Unit
	Jason E. Mattis	2616

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _1/30/07_.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1,3-5,7,8,10-14,16-19,21,23,24,26,27 and 29-33_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1, 3-5, 7, 8, 10-14, 16-19, 21, 23, 24, 26, 27, and 29-33_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1.   This Office Action is in response to the amendment filed 1/30/07. Due to the

amendment, the previous objection to claim 11 has been withdrawn. Claims 2, 6, 9, 15,

20, 22, 25, and 28 have been cancelled. Claims 1, 3-5, 7, 8, 10-14, 16-19, 21, 23, 24,

26, 27, and 29-33 are currently pending in the application.

Claim Rejections - 35 USC § 103

1.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

2.   Claims 1, 3-5, 7, 8, 11-14, and 16-19 are rejected under 35 U.S.C. 103(a) as

being unpatentable over Aiki et al. (U.S. Pat. 5410540) in view of Lipp et al. (U.S. Pat.

6751219 B1) and Sun et al. (U.S. Pat. 6574194 B1).

With respect to claim 1, Aiki et al. discloses a switching apparatus **(See**

column 3 lines 45-57 and Figure 1 of Aiki et al. for reference to switch 1, which is

a switching apparatus). Aiki et al. also discloses a first port coupled to receive an

input data frame **(See column 3 lines 45-57 and Figure 1 of Aiki et al. for reference**

to input ports L01 to L0N that receive cells, which are data frames). Aiki et al.

further discloses a first logic circuit coupled to receive the frame from the first port and

configured to determine a number of copies of the input data frame to make and to

make the number of copies **(See column 4 lines 12-39 and Figure 1 of Aiki et al. for**

reference to cell copy section 3, which is part of a logic circuit that is coupled to

receive an input frame and configured to determine a number of copies of the cell

to produce and to produce the copies). Aiki et al. also discloses a first memory

coupled to the first logic circuit and configured to store and read the copies **(See**

column 4 line 58 to column 5 line 6 and Figure 1 of Aiki et al. for reference to

buffer memory 4, which is coupled to the cell copy section 3, and is configured to

store and read the cell copies). Aiki et al. further discloses the memory comprising

multiple segments with each segment comprising multiple independently addressable

channels **(See column 4 line 58 to column 5 line 6 and Figure 1 of Aiki et al. for**

reference to memory addresses locations grouped into segments according to

output port number as allocated by a separate write address register for each

output port number and for reference to each of the write address registers

having multiple address locations, or channels, to store cells). Aiki et al. also

discloses reading multiple copies in a single read cycle **(See column 1 lines 35-61 of**

Aiki et al. for reference to distributing a broadcast cell to a plurality of output

ports in one output port designation cycle, which is a read cycle, irrespectively of

the number of output ports used for the broadcast operation). Aiki et al. further

discloses a second logic circuit coupled to the first memory and configured to determine

when to read at least one copy of the input data frame from the first memory **(See**

column 5 lines 7-20 and Figure 1 of Aiki et al. for reference to buffer memory

controller 6, which is a second logic circuit coupled to buffer memory 4,

configured to determine when to read a copy from the buffer memory 4). Aiki et al.

also discloses ports coupled to the first memory and configured to transmit the at least

one copy of the frame **(See column 5 liens 7-20 and Figure 1 of Aiki et al. for**

reference to output ports L91 to L9N, which are coupled to the buffer memory 4,

configured to transmit read copies of the cell). Aiki et al. further discloses that the

first logic circuit comprises a third logic circuit configured to determine one or more

empty locations in the first memory to store the copies of the input data frame **(See**

column 3 line 66 to column 4 line 12, column 4 line 58 to column 5 line 6 and

Figure 1 of Aiki et al. for reference to the buffer memory control section 6, which

is a third logic circuit that is part of the ATM switch 1, that determines idle

addresses, which are addresses of empty locations of the shared buffer memory

4, and stores the idle addresses in an idle address FIFO buffer 64 and for

reference using the idle addresses as addresses to store copies of input ATM

cells). Aiki et al. does not specifically disclose that the multiple ports are configured to

receive copies of the input data from the memory in parallel and to simultaneously

transmit copies of the input data frame. Although Aiki et al. does disclose the storing of

multiple copies of cells within the memory, Aiki et al. does not specifically disclose

determining a number of channels and segments or the amount of address space

needed to store the copies of data in the memory.

With respect to claim 14, Aiki et al. discloses a switching apparatus **(See column 3 lines 45-57 and Figure 1 of Aiki et al. for reference to switch 1, which is a switching apparatus)**. Aiki et al. also discloses a first logic circuit coupled to receive the frame and configured to determine a number of copies of the input data frame to make and to make the number of copies **(See column 4 lines 12-39 and Figure 1 of Aiki et al. for reference to cell copy section 3, which is part of a logic circuit that is coupled to receive an input frame and configured to determine a number of copies of the cell to produce and to produce the copies)**. Aiki et al. further discloses a memory coupled to the first logic circuit and configured to store and read the copies **(See column 4 line 58 to column 5 line 6 and Figure 1 of Aiki et al. for reference to buffer memory 4, which is coupled to the cell copy section 3, and is configured to store and read the cell copies)**. Aiki et al. also discloses the memory comprising multiple segments with each segment comprising multiple independently addressable channels **(See column 4 line 58 to column 5 line 6 and Figure 1 of Aiki et al. for reference to memory addresses locations grouped into segments according to output port number as allocated by a separate write address register for each output port number and for reference to each of the write address registers having multiple address locations, or channels, to store cells)**. Aiki et al. further discloses reading multiple copies in a single read cycle **(See column 1 lines 35-61 of Aiki et al. for reference to distributing a broadcast cell to a plurality of output ports in one output port designation cycle, which is a read cycle, irrespectively of the number of output ports used for the broadcast operation)**.

Aiki et al. also discloses a logic circuit coupled to the first memory and configured to

determine when to read at least one copy of the input data frame from the first memory

(See column 5 lines 7-20 and Figure 1 of Aiki et al. for reference to buffer memory

controller 6, which is a second logic circuit coupled to buffer memory 4,

configured to determine when to read a copy from the buffer memory 4). Aiki et al.

further discloses that the first logic circuit comprises a third logic circuit configured to

determine one or more empty locations in the memory to store the copies of the input

data frame **(See column 3 line 66 to column 4 line 12, column 4 line 58 to column 5**

line 6 and Figure 1 of Aiki et al. for reference to the buffer memory control section

6, which is a third logic circuit that is part of the ATM switch 1, that determines

idle addresses, which are addresses of empty locations of the shared buffer

memory 4, and stores the idle addresses in an idle address FIFO buffer 64 and for

reference using the idle addresses as addresses to store copies of input ATM

cells). Aiki et al. does not specifically disclose that the multiple ports are configured to

receive copies of the input data from the memory in parallel and to simultaneously

transmit copies of the input data frame. Although Aiki et al. does disclose the storing of

multiple copies of cells within the memory, Aiki et al. does not specifically disclose

determining a number of channels and segments or the amount of address space

needed to store the copies of data in the memory.

      With respect to claims 1 and 14, Lipp et al., in the field of communications

discloses multiple ports configured to receive copies of input data from a memory in

parallel and to simultaneously transmit copies of the input data frame **(See column 8**

line 61 to column 9 line 34 of Lipp et al. for reference to replicating a input data of a multicast packet, storing the replicated data, and transmitting the replicated data though multiple egress ports in parallel to simultaneously transmit the copies). Using multiple ports configured to receive copies of input data from a memory in parallel and to simultaneously transmit copies of the input data frame has the advantage of allowing multiple output ports to transmit data at the same time without having to wait for other output ports to finish transmission.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Lipp et al. to combine using multiple ports configured to receive copies of input data from a memory in parallel and to simultaneously transmit copies of the input data frame, as suggested by Lipp et al., with the system and method of Aiki et al., with the motivation being to allow multiple output ports to transmit data at the same time without having to wait for other output ports to finish transmission.

With respect to claims 7 and 18, Aiki et al. discloses the third logic circuit configured to determine how many additional ports will output copies of the frame **(See column 4 lines 12-39 and Figure 1 of Aiki et al. for reference to cell copy section 3 containing copy information table 34, which is used to determine the number of copies of the cell to make).** The combination of Aiki et al. and Lipp et al. does not specifically disclose calculating the amount of storage space needed to store the copies.

With respect to claims 8 and 19, the combination of Aiki et al. and Lipp et al. does not disclose determining the size of the frame and calculating the space necessary for storage.

With respect to claims 1, 7, 8, 14, 18, and 19, Sun et al., in the field of communications, discloses determining the size of a date frame and determining how many address locations are needed for the frame **(See column 4 lines 58-64, column 6 line 64 to column 7 line 30 and Figures 2, 3A, and 3B of Sun et al. for reference to receiving variable length packets and determining how much storage is needed for the packets based on the size of the packets)**. Determining the size of a date frame and determining how many address locations are needed for the frame has the advantage of allowing the size of data frames to be variable and providing more flexibility in the amount of data transmitted.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Sun et al., to combine determining the size of a date frame and determining how many address locations are needed for the frame, as suggested by Sun et al., with the system and method of Aiki et al. and Lipp et al., with the motivation being to allow the size of data frames to be variable and to provide more flexibility in the amount of data transmitted.

With respect to claim 3, Aiki et al. discloses a second memory configured to keep track of all the empty locations in the first memory **(See column 3 line 66 to column 4 line 12, column 4 line 58 to column 5 line 6 and Figure 1 of Aiki et al. for**

reference to idle address FIFO buffer 64, which is a second memory stores
addresses of empty locations in the buffer memory 4).

With respect to claims 4, 5, 16, and 17, Aiki et al. discloses a third logic circuit
determining where there are empty memory locations **(See column 3 line 66 to
column 4 line 12, column 4 line 58 to column 5 line 6 and Figure 1 of Aiki et al. for
reference to the control section 6 having logic to determine an empty location of
write address registers corresponding to output port numbers in the buffer
memory 4 by using buffer 64).**

With respect to claim 11, Aiki et al. discloses a bus coupled with the first
memory and transmitting ports to transmit data including the copy from the memory to
the transmitting ports **(See Figure 1 of Aiki et al. for reference to a bus L4
connecting the buffer memory 4 with the output ports L91 to L9N such that data
is transmitted on the bus L4 from the memory 4 to the ports L91 to L9N).**

With respect to claim 12, Aiki et al. discloses logic circuit configured to select at
least one copy from the bus **(See column 5 lines 7-20 and Figure 1 of Aiki et al. for
reference to output select decoder 65, which is a logic circuit, configured to
select an copy of data to output on the bus to the output port).**

With respect to claim 13, Aiki et al. discloses that an output control logic circuit
is configured to indicate a location in the first memory where an associated transmitting
port is to obtain the frame **(See column 5 lines 7-20 and Figure 1 of Aiki et al. for
reference to buffer control section 6 including logic configured to determine
where in the buffer memory 4 the data to be output to an output port is stored).**

3.   Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aiki et

al. in view of Lipp et al. and Sun et al. and in further view of Medina et al. (U.S.

Publication US 2005/0041579 A1).

With respect to claim 10, the combination of Aiki et al., Lipp et al., and Sun et

al. does not disclose that the memory is distributed across the switching apparatus.

With respect to claim 10, Medina et al., in the field of communications,

discloses using a distributed memory in a switch **(See page 2 paragraphs 19-21 and**

Figure 2 of Medina et al. for reference to the memory being distributed with each

port having a dedicated output port). Using a distributed memory in a switch has the

advantage of allowing each output port to have a dedicated amount of memory such

that if data congestion occurs at one output port, the memory of the other output ports is

not affected.

It would have been obvious for one of ordinary skill in the art at the time of the

invention, when presented with the work of Medina et al., to combine using a distributed

memory in a switch, as suggested by Medina et al., with the system and method of Aiki

et al., Lipp et al., and Sun et al., with the motivation being to allow allowing each output

port to have a dedicated amount of memory such that if data congestion occurs at one

output port, the memory of the other output ports is not affected.

4.   Claims 21, 23, 24, 26, 27, and 29-33 are rejected under 35 U.S.C. 103(a) as

being unpatentable over Aiki et al. in view of Lipp et al., Sun et al., and Moy-Yee et al.

(U.S. Pat. 6724761).

With respect to claim 21, Aiki et al. discloses a switching apparatus **(See**

column 3 lines 45-57 and Figure 1 of Aiki et al. for reference to switch 1, which is

a switching apparatus). Aiki et al. also discloses a first port coupled to receive an

input data frame **(See column 3 lines 45-57 and Figure 1 of Aiki et al. for reference**

to input ports L01 to L0N that receive cells, which are data frames). Aiki et al.

further discloses a memory coupled to the first logic circuit and configured to store and

read the copies **(See column 4 line 58 to column 5 line 6 and Figure 1 of Aiki et al.**

for reference to buffer memory 4, which is coupled to the cell copy section 3, and

is configured to store and read the cell copies). Aiki et al. further discloses the

memory comprising multiple segments with each segment comprising multiple

independently addressable channels **(See column 4 line 58 to column 5 line 6 and**

Figure 1 of Aiki et al. for reference to memory addresses locations grouped into

segments according to output port number as allocated by a separate write

address register for each output port number and for reference to each of the

write address registers having multiple address locations, or channels, to store

cells). Aiki et al. also discloses a logic circuit coupled to receive the frame from the first

port and configured to determine a number of copies of the input data frame to make

and to make the number of copies **(See column 4 lines 12-39 and Figure 1 of Aiki et**

al. for reference to cell copy section 3, which is a logic circuit that is coupled to

receive an input frame and configured to determine a number of copies of the cell to produce and to produce the copies). Aiki et al. also discloses reading multiple copies in a single read cycle **(See column 1 lines 35-61 of Aiki et al. for reference to distributing a broadcast cell to a plurality of output ports in one output port designation cycle, which is a read cycle, irrespectively of the number of output ports used for the broadcast operation).** Aiki et al. further discloses a logic circuit coupled to the first memory and configured to determine when to read at least one copy of the input data frame from the first memory **(See column 5 lines 7-20 and Figure 1 of Aiki et al. for reference to buffer memory controller 6, which is a logic circuit coupled to buffer memory 4, configured to determine when to read a copy from the buffer memory 4).** Aiki et al. also discloses a transmitting ports coupled to the first memory and configured to transmit the copies of the frame **(See column 5 liens 7-20 and Figure 1 of Aiki et al. for reference to output ports L91 to L9N, which are coupled to the buffer memory 4, configured to transmit read copies of the cell).** Aiki et al. further discloses a third logic circuit configured to determine one or more empty locations in the memory to store the copies of the input data frame **(See column 3 line 66 to column 4 line 12, column 4 line 58 to column 5 line 6 and Figure 1 of Aiki et al. for reference to the buffer memory control section 6, which is a third logic circuit that is part of the ATM switch 1, that determines idle addresses, which are addresses of empty locations of the shared buffer memory 4, and stores the idle addresses in an idle address FIFO buffer 64 and for reference using the idle addresses as addresses to store copies of input ATM cells).** Aiki et

al. does not specifically disclose that the multiple ports are configured to receive copies

of the input data from the memory in parallel and to simultaneously transmit copies of

the input data frame. Although Aiki et al. does disclose the storing of multiple copies of

cells within the memory, Aiki et al. does not specifically disclose determining a number

of channels and segments or the amount of address space needed to store the copies

of data in the memory. Aiki et al. does not disclose that the logic circuits are embodied

as a processor.

With respect to claim 29, Aiki et al. discloses a switching apparatus **(See**

column 3 lines 45-57 and Figure 1 of Aiki et al. for reference to switch 1, which is

a switching apparatus). Aiki et al. also discloses determining a number of copies of

the input data frame to make and generating the number of copies **(See column 4 lines**

12-39 and Figure 1 of Aiki et al. for reference to cell copy section 3, which is a

logic circuit that is coupled to receive an input frame and configured to determine

a number of copies of the cell to produce and to produce the copies). Aiki et al.

further discloses determining one or more empty locations in the memory **(See column**

4 line 58 to column 5 line 6 and Figure 1 of Aiki et al. for reference to the control

section 6 having logic to determine an empty location in the buffer memory 4 by

using buffer 64). Aiki et al. also discloses forwarding instructions and data to the

memory to store the copies in the memory **(See column 4 line 58 to column 5 line 6**

and Figure 1 of Aiki et al. for reference to buffer memory 4, which is coupled to

the cell copy section 3, and is configured to store copies based on instructions).

Aiki et al. further discloses forwarding instructions to the memory to read out copies of

the input data frame from the first memory **(See column 5 lines 7-20 and Figure 1 of**

Aiki et al. for reference to buffer memory controller 6, which is a second logic

circuit coupled to buffer memory 4, configured to determine when to read a copy

from the buffer memory 4). Aiki et al. also discloses reading multiple copies in a

single read cycle **(See column 1 lines 35-61 of Aiki et al. for reference to**

distributing a broadcast cell to a plurality of output ports in one output port

designation cycle, which is a read cycle, irrespectively of the number of output

ports used for the broadcast operation). Aiki et al. also discloses forwarding

instructions to multiple transmitting ports causing the ports to receive and to transmit the

copies of the frame **(See column 5 liens 7-20 and Figure 1 of Aiki et al. for reference**

to output ports L91 to L9N, which are coupled to the buffer memory 4, configured

to transmit read copies of the cell). Aiki et al. further discloses determining one or

more empty locations in the memory to store the copies of the input data frame **(See**

column 3 line 66 to column 4 line 12, column 4 line 58 to column 5 line 6 and

Figure 1 of Aiki et al. for reference to the buffer memory control section 6, which

is a third logic circuit that is part of the ATM switch 1, that determines idle

addresses, which are addresses of empty locations of the shared buffer memory

4, and stores the idle addresses in an idle address FIFO buffer 64 and for

reference using the idle addresses as addresses to store copies of input ATM

cells). Aiki et al. does not specifically disclose that the multiple ports are configured to

receive copies of the input data from the memory in parallel and to simultaneously

transmit copies of the input data frame. Although Aiki et al. does disclose the storing of

multiple copies of cells within the memory, Aiki et al. does not specifically disclose determining a number of channels and segments or the amount of address space needed to store the copies of data in the memory. Aiki et al. does not disclose that the logic circuits are embodied as a processor.

With respect to claims 21 and 29, Lipp et al., in the field of communications discloses multiple ports configured to receive copies of input data from a memory in parallel and to simultaneously transmit copies of the input data frame **(See column 8 line 61 to column 9 line 34 of Lipp et al. for reference to replicating a input data of a multicast packet, storing the replicated data, and transmitting the replicated data though multiple egress ports in parallel to simultaneously transmit the copies)**. Using multiple ports configured to receive copies of input data from a memory in parallel and to simultaneously transmit copies of the input data frame has the advantage of allowing multiple output ports to transmit data at the same time without having to wait for other output ports to finish transmission.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Lipp et al. to combine using multiple ports configured to receive copies of input data from a memory in parallel and to simultaneously transmit copies of the input data frame, as suggested by Lipp et al., with the system and method of Aiki et al., with the motivation being to allow multiple output ports to transmit data at the same time without having to wait for other output ports to finish transmission.

With respect to claims 26, Aiki et al. discloses the determining how many ports will output copies of the frame **(See column 4 lines 12-39 and Figure 1 of Aiki et al. for reference to cell copy section 3 containing copy information table 34, which is used to determine the number of copies of the cell to make).** The combination of Aiki et al. and Lipp et al. does not specifically disclose calculating the amount of storage space needed to store the copies.

With respect to claim 27, the combination of Aiki et al. and Lipp et al. does not disclose determining the size of the frame and calculating the space necessary for storage.

With respect to claim 28, the combination of Aiki et al. and Lipp et al. does not disclose determining how many addressable locations are needed to store the copies of the frame.

With respect to claim 33, the combination of Aiki et al. and Lipp et al. does not disclose determining the size of received data and determining where to store the received data.

With respect to claims 21, 26-29, and 33, Sun et al., in the field of communications, discloses determining the size of a date frame and determining how many address locations are needed for the frame **(See column 4 lines 58-64, column 6 line 64 to column 7 line 30 and Figures 2, 3A, and 3B of Sun et al. for reference to receiving variable length packets and determining how much storage is needed for the packets based on the size of the packets).** Determining the size of a date frame and determining how many address locations are needed for the frame has

the advantage of allowing the size of data frames to be variable and providing more

flexibility in the amount of data transmitted.

It would have been obvious for one of ordinary skill in the art at the time of the

invention, when presented with the work of Sun et al., to combine determining the size

of a date frame and determining how many address locations are needed for the frame,

as suggested by Sun et al., with the system and method of Aiki et al. and Lipp et al.,

with the motivation being to allow the size of data frames to be variable and to provide

more flexibility in the amount of data transmitted.

With respect to claims 21 and 29, Moy-Yee et al. discloses using a

microprocessor and software on a computer readable medium to store and execute

instructions for operating a switching apparatus **(See column 5 lines 44-51 of Moy-Yee**

et al. for reference to using a microprocessor and software). Using a

microprocessor and software on a computer readable medium to store and execute

instructions for operating a switching apparatus has the advantage of allowing the

system instructions to be written in software such that it is easy to reconfigure new

instructions without changing the hardwiring of the apparatus.

It would have been obvious for one of ordinary skill in the art at the time of the

invention, when presented with the work of Moy-Yee et al., to combine using a

microprocessor and software on a computer readable medium to store and execute

instructions for operating a switching apparatus with the system and method of Aiki et

al., Sun et al., and Lipp et al., with the motivation being to allow the system instructions

to be written in software such that it is easy to reconfigure new instructions without changing the hardwiring of the apparatus.

With respect to claims 23, 24, and 30, Aiki et al. discloses a third logic circuit determining where there are empty memory locations **(See column 4 line 58 to column 5 line 6 and Figure 1 of Aiki et al. for reference to the control section 6 having logic to determine an empty location in the buffer memory 4 by using buffer 64)**.

With respect to claim 31, the combination of Aiki et al. discloses storing the copies in multiple segments **(See column 4 line 58 to column 5 line 6 and Figure 1 of Aiki et al. for reference to storing copies in memory addresses locations grouped into segments according to output port number as allocated by a separate write address register for each output port number and for reference to each of the write address registers having multiple address locations, or channels, to store cells)**.

With respect to claim 32, Aiki et al. discloses that when the memory reads out one copy, the memory also reads out a previously stored copy of a previously received frame **(See column 1 lines 35-61 of Aiki et al. for reference to distributing a broadcast cell as well as other cells to a plurality of output ports in one output port designation cycle, which is a read cycle, irrespectively of the number of output ports used for the broadcast operation)**.

Response to Arguments

5.   Applicant's arguments with respect to claims 1, 3-5, 7, 8, 10-14, 16-19, 21, 23,

24, 26, 27, and 29-33 have been considered but are moot in view of the new ground(s)

of rejection.

Conclusion

6.   The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure. Ganmukhi et al. (U.S. Pat. 5548588) discloses another system

and method for multicasting data cells.

7.   Applicant's amendment necessitated the new ground(s) of rejection presented in

this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37

CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Jason E. Mattis whose telephone number is (571) 272-

3154. The examiner can normally be reached on M-F 8AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

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